340KHz, 36V/2.5A Step-down Converter With Soft-Start

General Description

The LP6482S contains an independent 340KHz constant frequency, current mode, PWM step-down converters. The converter integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. The converter can supply 2500mA of load current. The LP6482S can also run at 90% duty cycle for low dropout applications.

It provides fast transient response and cycle-by-cycle limit with current mode control. And adjustable soft start prevents inrush current at turn on and the supply current drops below 0.1uA in shutdown mode.

The LP6482S is available in a SOP8 and ESOP8 package and is rated over the -40°C to 85°C temperature range.

Features

- Input Voltage Range: 4.5V to 36V
- Output Voltage Range: 0.6V to 12V
- 2500mA Load Current (LP6482SSPF)
- Up to 96% Efficiency
- <6uA Shutdown Current
- 340KHz Switching Frequency
- Short Circuit Protection
- Thermal Fault Protection
- SOP8 Package
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Portable Media Players
- Cellular and Smart mobile phone
- PDA/DSC
- GPS Applications

Order Information

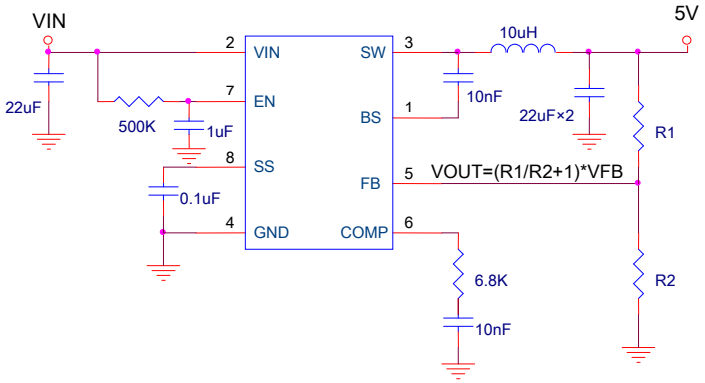
LP6482S □ □ □

- F: Pb-Free
- Package Type
  - SO: SOP8
  - SP: ESOP-8

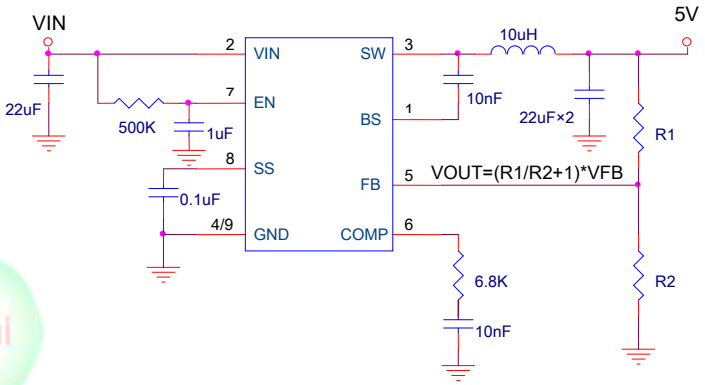
Marking Information

Device	Marking	Package	Shipping
LP6482S	LPS LP6482S YWX	SO:SOP-8 SP:ESOP-8	3K/REEL
Y: Year code. W: Week code. X: Batch numbers.			

Typical Application Circuit

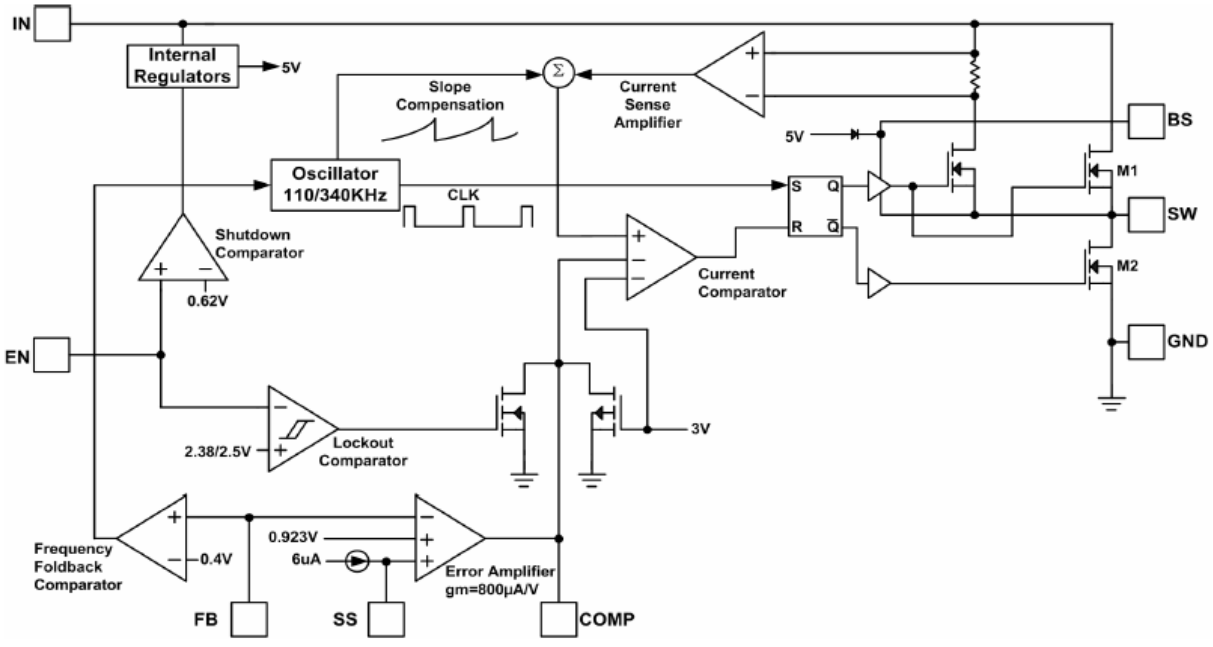


LP6482S(SOP-8) application circuit

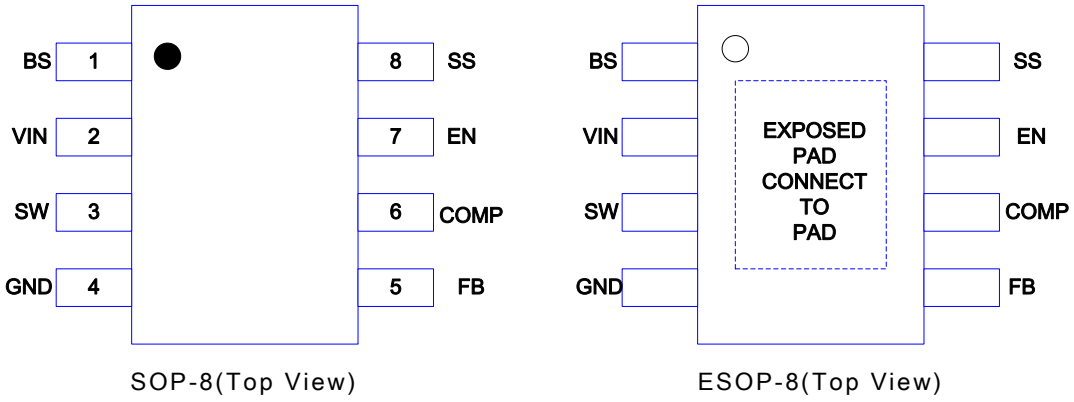


LP6482S(ESOP-8) application circuit

Function Diagram



Functional Pin Description

Package Type	Pin Configurations
SOP-8 / ESOP-8	

Pin Description

Pin	Name	Description
1	BS	High-Side Gate Drive Boost Input. Connect a 0.01uF or greater capacitor from SW to BS to power the high side switch.
2	VIN	Supply Input.
3	SW	Switch Mode Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
4	GND	Ground.
5	FB	Feedback Input. Connect FB to the center point of the external resistor divider. Normal voltage for this pin is 0.923V.
6	COMP	Loop compensation input. Connect a series RC network from COMP to GND to Compensate the regulation control loop.
7	EN	Enable Control Input. Drive EN above 2.5V to turn on the Channel. Drive EN below 0.4V to turn it off (shutdown current < 0.1μA).
8	SS	Soft-start control input. Connect an external capacitor to program the soft-start. If unused, leave it open, which means internal soft-start function.
9	E-Pad	Exposed Pad. The pin connect to GND.

Absolute Maximum Ratings Note 1

- ✧ Input Voltage to GND ---------- 36V
- ✧ SW\BS to GND (VSW) ---------- -0.3V to V_{IN} +0.3V
- ✧ FB to GND (VFB) ---------- -0.3V to 6V
- ✧ EN to GND (VEN) ---------- -0.3V to 6V
- ✧ COMP\SS to GND (VEN) ---------- -0.3V to 6V
- ✧ Junction Temperature ---------- 150°C
- ✧ Storage Temperature ---------- -65℃ to 165℃
- ✧ Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- 260℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (SOP8, P_D,T_A=25°C) ---------- 1.5W
- ✧ Thermal Resistance (SOP8, θ_{JA}) ---------- 80℃/W
- ✧ Maximum Power Dissipation (ESOP8, P_D,T_A=25°C) ---------- 2W
- ✧ Thermal Resistance (ESOP8, θ_{JA}) ---------- 50℃/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) ---------- 2KV
- ✧ MM(Machine Mode) ---------- 200V

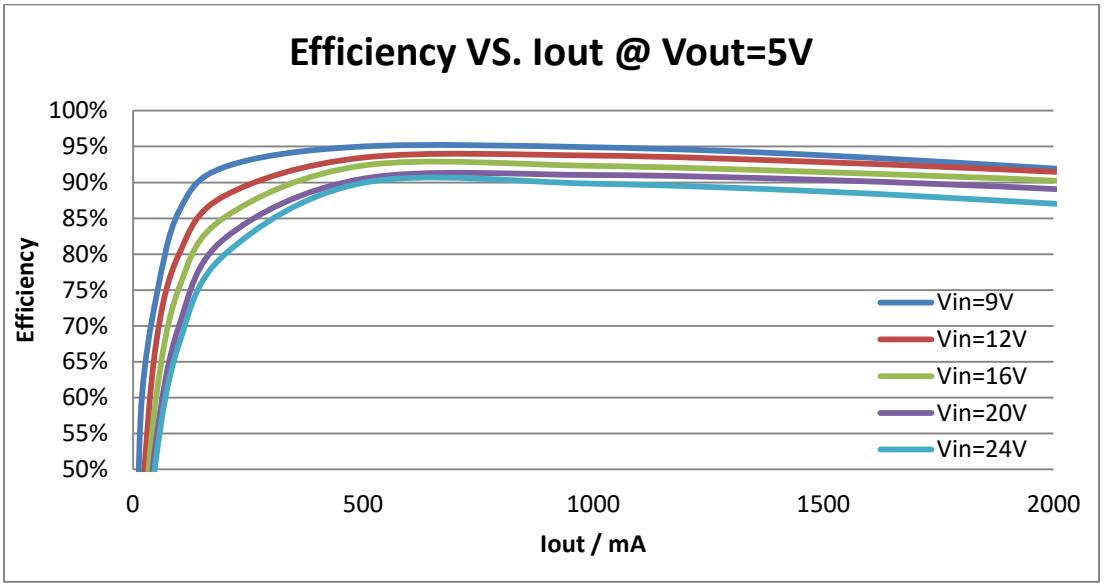
Electrical Characteristics

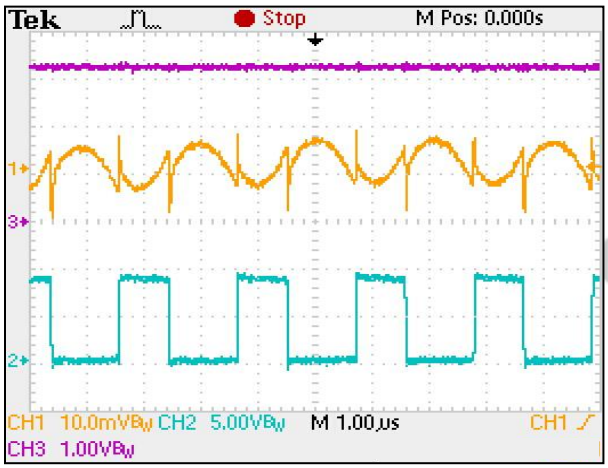
V_{IN}=12V, V_{EN}=5V, T_A=25℃, unless otherwise noted

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIN	Input Voltage		4.5		36	V
ΔV_{OUT}	Output Voltage Line Regulation	I_{LOAD}=1mA to 2000mA		0.3	0.6	%/V
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN}=5V to 30V, V_{EN}=5V		0.25	0.4	%/V
V_{OUT}	Output Voltage Range		0.923		12	V
I_Q	Quiescent Current	V_{IN}=12V			15	mA
I_{SHDN}	Shutdown Current	EN=GND			1	μA
I_{LIM}	P-Channel Current Limit		3			A
$R_{DS(ON)\_H}$	High-Side Switch On Resistance			85		mΩ
$R_{DS(ON)\_L}$	Low-Side Switch On Resistance			80		mΩ
I_{LX_LEAK}	LX Leakage Current	V_{EN}=0V, V_{SW}=0 or 5V, V_{IN}=5V		1		μA
V_{FB}	Feedback Threshold Voltage Accuracy	V_{IN}=12V	0.895	0.923	0.951	V
I_{FB}	FB Leakage Current	V_{OUT}=5.0V			30	nA
f_{OSC}	Oscillator Frequency			340		KHz
t_S	Startup Time	From Enable to Output Regulation		120		μs
T_{SD}	Over-Temperature Shutdown Threshold			150		℃
T_{HYS}	Over-Temperature Shutdown Hysteresis			20		℃
$V_{EN(L)}$	Enable Threshold Low				0.4	V
$V_{EN(H)}$	Enable Threshold High		2.5		6	V
I_{EN}	Input Low Current	V_{IN}=12V, V_{EN}=5V		1		μA

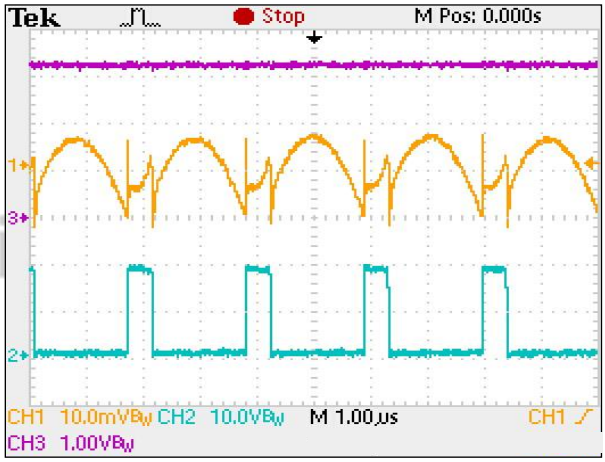
Note: Output Voltage: $V_{OUT} = V_{FB} \times (1 + R_1 / R_2)$ Volts;

Typical Operating Characteristics





V_{IN}=24V, V_{OUT}=5V, I_{OUT}=1.5A



V_{IN}=24V, V_{OUT}=5V, I_{OUT}=2.0A

Application Information

The LP6482S is current-mode step-down switching regulator. The device regulates an output voltage as low as 0.923V. The device can provide continuous current up to 2.5A to the output with V_{IN}=12V. The LP6482S uses current-mode architecture to control the regulator loop. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal error amplifier. The output current of the trans-conductance error amplifier is presented at COMP pin where a RC network compensates the regulator loop. Slope compensation is added to eliminate sub harmonic oscillation at high duty cycle. The slope compensation adds voltage ramp to the inductor current signal which reduces maximum inductor peak current at high duty cycles.

The device uses an internal H_side N-channel switch to step down the input voltage to the regulated output voltage. Since the H_side n-channel switch requires gate voltage greater than the input voltage, a boost BS capacitor is connected between SW and BS to drive the n-channel gate. The BS capacitor is internally charged while the switch is off. An internal 6.8Ω switch from SW to GND is added to insure that SW is pulled to GND when the switch is off to fully charge the BS capacitor.

Setting the Output Voltage

The output voltage is set through a resistive voltage divider. The voltage divider divides the output voltage down by the ratio:

$$V_{FB}=V_{OUT}\times R2/(R1+R2)=0.923V$$

Thus the output voltage is:

$$V_{OUT}=0.923V\times(1+R1/R2)$$

Inductor Selection

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current and lower output ripple voltage. However, the larger value inductor has a larger physical size, higher series resistance, and lower saturation current. Choose an inductor that does not saturate under the worst-case load conditions. A good rule for determining the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. The inductance value can be calculated by the equation:

$$L=(V_{OUT})\times(V_{IN}-V_{OUT})/(V_{IN}\times f\times\Delta I)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f is the switching frequency, and ΔI is the peak-to-peak inductor ripple current.

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore an input capacitor C_{IN} is required to supply the AC current to the step-down converter while maintaining the DC input voltage. A low ESR capacitor is required to keep the noise minimum at the IC. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. The input capacitor value should be greater than 22μF, and the RMS current rating should be greater than approximately 1/2 of the DC load current. For insuring stable operation C_{IN} should be placed as close to the IC as possible. Alternately a smaller high quality ceramic 0.1μF capacitor may be placed closer to the IC and a larger capacitor placed further away. Using this technique, it is recommended that the larger capacitor type are either tantalum or electrolytic. All ceramic capacitors should be placed close to the LP6482S.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. The characteristics of the output capacitor also affect the stability of the regulator control loop. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is estimated to be:

$$V_{RIPPLE}=1.4\times V_{IN}\times(f_{LC}/f)^2$$

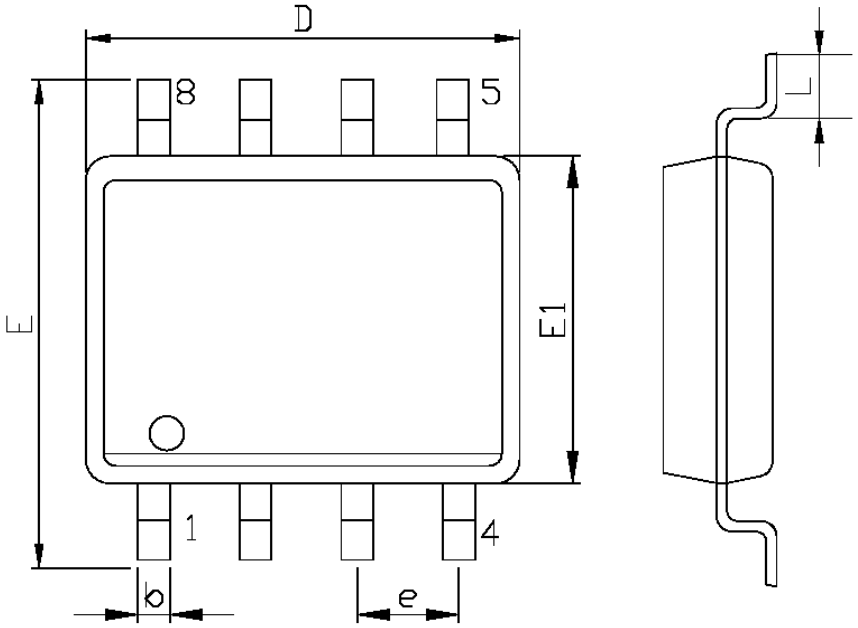
Where V_{RIPPLE} is the output ripple voltage, V_{IN} is the input voltage, f_{LC} is the resonant frequency of the LC filter, f is the switching frequency. In the case of tantalum or low ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is calculated as:

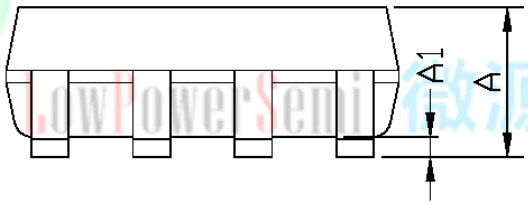
$$V_{RIPPLE}\approx\Delta I\times R_{ESR}$$

Where V_{RIPPLE} is the output voltage ripple, ΔI is the inductor ripple current, and R_{ESR} is the equivalent series resistance of the output capacitors.

Packaging Information

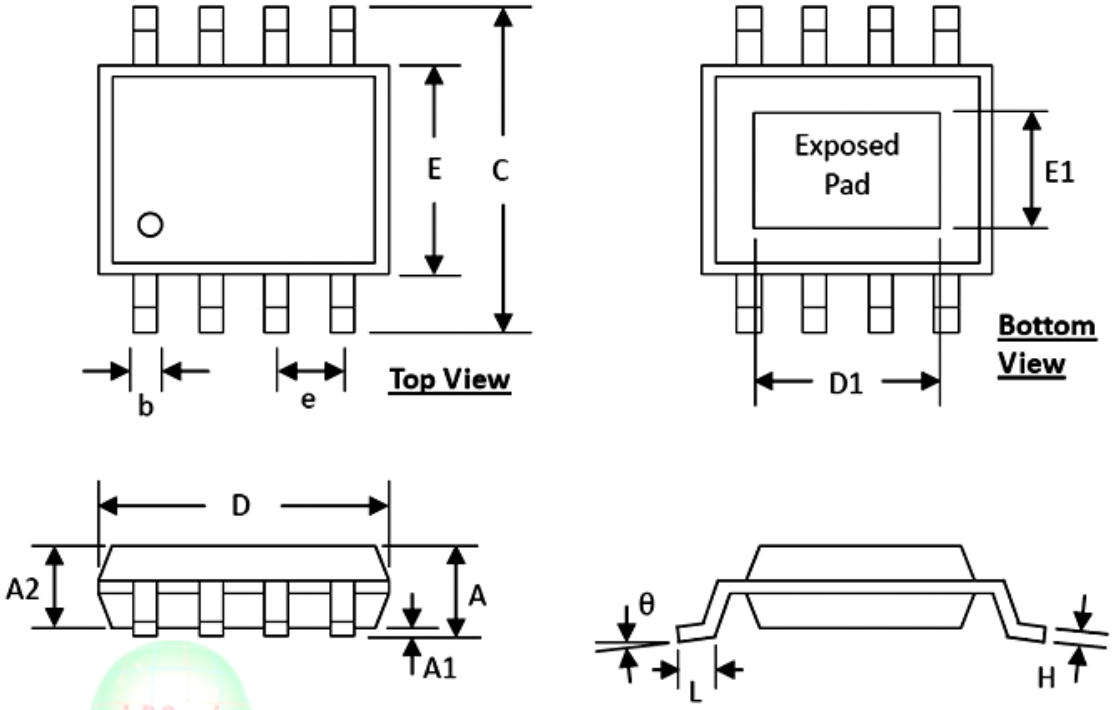
SOP8





SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E	5.80	6.20	0.228	0.244
E1	3.90		0.153	
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	

ESOP8



SYMBOLS	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A	1.30	1.70	0.051	0.067
A1	0.00	0.15	0.000	0.006
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
C	5.80	6.20	0.228	0.244
D	4.80	5.00	0.189	0.197
D1	3.15	3.45	0.124	0.136
E	3.80	4.00	0.150	0.157
E1	2.26	2.56	0.089	0.101
e	1.27 BSC		0.050 BSC	
H	0.19	0.25	0.0075	0.0098
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°